

## Claims

- [c1] An integrated circuit including a field effect transistor (FET) comprising:  
a gate conductor having an even number of fingers disposed between alternating source and drain regions of a substrate, said fingers being disposed in a pattern over an area of said substrate having a length in a horizontal direction, said area equaling said length multiplied by a width in a vertical direction occupied by an odd number of said fingers.
- [c2] The integrated circuit of claim <sup>1</sup>~~2~~ wherein said width is a minimum width for providing said odd number of fingers within the integrated circuit. *AK*  
*5/6/04*
- [c3] The integrated circuit of claim 1 wherein said FET is a first FET of a column of said FETs including said first FET and a second FET disposed adjacent to said first FET, wherein a source region of said first FET is shared with a source region of said second FET.
- [c4] The integrated circuit of claim 1 wherein said FET is a first FET of a column of said FETs including said first FET and a second FET disposed adjacent to said first FET,